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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,371	JOHNSON, LEITH	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *6,7,12,13,22,24 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-11,14-21,23, 25 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Amendments and Remarks filed on February 10, 2006 regarding application 10/017,371 filed on December 7, 2001.

2. Claims 1, 8, 14, 18, 23 and 25 have been amended.

Claims 6-7, 12-13, 22, 24 and 26 have been canceled.

Claims 27-31 have been added.

Claims 1-5, 8-11, 14-21, 23, 25 and 27-31 are pending in the application under consideration.

3. ***Response to Remarks and Amendments***

Applicants' remarks and amendments have been fully and carefully considered.

Claims 1, 8, 14, 18, 23 and 25 have been amended to include the additional limitations of "**wherein the mapping defines a non-monotonic function**."

In response to these amendments, another iteration of claim analysis, based on the previously relied on references (Gulick et al., US 6,314,501; Vishin et al., US 5,860,146), and particularly addressing the newly amended limitation, has been embarked. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 8-11, 14-21, 23, 25 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick et al. (US 6,314,501), and in view of Vishin et al. (US 5,860,146).

As to claim 1, Gulick et al. disclose **in a partitionable computer system** [Computer System and method for Operating Multiple Operating systems in Different partitions of the Computer System and for Allowing the Different Partitions to Communicate with One Another through Shared Memory (title)] **including a plurality of machine resources having a plurality of machine resource identifiers** [the corresponding a plurality of machine resources is the plurality of memory storage unit (figure 2, 220A~220D) which form the main memory (figure 1, 160) of the computer system (figure 1, 100). Each one of the plurality of Memory Storage Unit (MSU) has its own address space (i.e., the identifier) as shown in figure 3], **a method for creating a physical resource identifier space in a partition of the partitionable computer system** [figure 3 shows a plurality of partitions and how their physical address spaces are related to the MSU address space], **the method comprising steps of**:
(A) **establishing a mapping** [figure 3 shows the address mapping between 4 instances of partitions and a MSU] **between a plurality of physical resource identifiers** [figure 3 shows 4 instances of partitions and their associated physical resource identifiers] **and at least some of the plurality of machine resource identifiers** [figure 3 also shows the machine resource associated with the MSU] **using**

a content address memory [see below], **wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero** [the address space of each of the partition always begins at address zero (column 14, lines 48-67); figure 5]; **and wherein the mapping defines a non-monotonic function** [FIG. 33 is a block diagram of apparatus for carrying out the address relocation and reclamation methods of the present invention which leads to a non-monotonic mapping function from physical to machine resources; FIG. 33 is a block diagram illustrating apparatus, in the form of registers and logic, for performing the relocation and reclamation functions described above, in accordance with the preferred embodiment. This logic is provided in each TCT 270 to perform the relocation and reclamation functions of the present invention for memory addresses issued by the processors (MP) 240 interfaced to the TCT 270. As mentioned, this logic is also replicated in each TCM 285 in order to perform relocation and reclamation for memory addresses issued by an I/O processor via a respective DIB 250. According to the preferred embodiment, as illustrated in FIG. 33, a memory address issued on the address lines of a given processor 240 (or by an I/O processor via a respective DIB 250) is captured in a Processor_Address register 3310. In the preferred embodiment, main memory is addressable in words of 8 bytes bits (1 word=8 bytes=64 bits), and therefore, the least significant 3 bits of the processor address are not needed for generating an adjusted address. Thus, as shown, only bits [35:3] are captured in the Processor_Address register 3310. Furthermore, in the preferred embodiment, main memory is cached in blocks of eight (8) words (8 words=64 bytes), and thus bits [35:6] represent the effective cache block address. As

shown, these bits are captured in a subsequent Cache_Block_Address register 3312 (column 19, lines 24-49)]; **and**

(B) **providing, to an operating system** [column 2, lines 37-43; column 2, lines 46-50; column 3, lines 1-5; figure 22; column 8, lines 47-57] **executing in the partition** [the operating system (column 14, lines 48-67); figure 3], **an interface for the operating system to access the at least some of the plurality of machine resources using the plurality of physical resource identifiers as indices into the content address memory** [figures 4 and 5; column 16, lines 30-67; see below].

Regarding claim 1, Gulick et al. do not teach **establishing the mapping between the physical resource identifiers and the machine resource identifiers using a content addressable memory, and using the plurality of physical resource identifiers as indices into the content address memory**.

However, the subject matter of content addressable memory is well known and is widely adopted in a computer system to reduce memory access latency and to increase operational speed (see Microsoft Computer Dictionary, 5th edition, Microsoft Press, 2002, page 125 – content-addressed storage).

Further, Vishin et al. teach in their invention "Auxiliary Translation Lookaside Buffer for Assisting in Accessing Data in Remote Address Space" a method and apparatus of translating virtual addresses into physical address using a remote translation lookaside buffer (RTLB) which is implemented using a content addressable memory [figure 5 shows the translation and mapping between virtual addresses and physical addresses (column 4, lines 41-62); figure 6 shows that a CAM is used to

implement a remote translation lookaside buffer (RTLB); column 4, lines 63-67; column 5, lines 1-20], and the association of the physical resource identifiers and the indices of the CAM [figure 6; column 5, lines 60-67; column 4, lines 5-10; column 5, lines 32-59; column 6, lines 1-35].

A content addressable memory allows entries in a storage device to be searched and a target be identified in an efficient manner, hence reducing memory access latency and improving system throughput.

Therefore, it would be obvious for ones of ordinary skills in the art at the time of Applicant's invention to recognize the benefit offered by a content addressable memory, as demonstrated by Vishin et al., and to incorporate it into the existing apparatus disclosed by Gulick et al. to further enhance the performance of the system.

As to claim 2, Gulick et al. disclose that **the plurality of machine resources** [the corresponding a plurality of machine resources is the plurality of memory storage unit (figure 2, 220A~220D) which form the main memory (figure 1, 160) of the computer system (figure 1, 100)] **comprises a plurality of machine memory locations** [figures 3 and 5 show the MSU memory space; figure 7 shows the case of multiple MSUs], **wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses** [figures 5, 6, and 7], **and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses** [figure 5 shows 3 instances of partitions and their associated physical address space].

As to claim 3, Gulick et al. disclose that **the method of claim 1 further comprising a step of performing the steps (A) and (B) for each of a plurality of partitions of the partitionable computer** [figure 5 shows that steps (A) and (B) are performed for all 3 partitions.

As to claim 4, Gulick et al. disclose that **the step (A) comprises a step of creating an address translation table that records the mapping between the plurality of physical resource identifiers and the at least some of the plurality of machine resource identifiers** [figures 4 and 5; Each TCT 270 performs address relocation, reclamation, and translation for memory addresses issued by the processors to which it is connected, as described more fully below (column 11, lines 51-54); column 22, lines 9-67].

As to claim 5, Gulick et al. disclose that **the interface comprises means for translating a physical resource identifier selected from among the plurality of physical resource identifiers into one of the plurality of machine resource identifiers in accordance with the mapping** [figures 4 and 5; column 22, lines 9-67].

As to claim 8, refer to "As to claim 1."

As to claim 9, refer to "As to claim 2."

As to claim 10, refer to "As to claim 4."

As to claim 11, refer to "As to claim 5."

As to claim 14, refer to "As to claim 1" through "As to claim 5." Further, Gulick et al. disclose that [The TCT 270 takes a processor's memory read/write address (after any relocation and/or reclamation) and passes it through an address translation

function (column 23, lines 7-23). Hence, the desired data resides in the machine resource is accessed for read or write operations using the translated address].

As to claim 15, refer to "As to claim 2."

As to claims 16-17, Gulick et al. disclose that [The TCT 270 takes a processor's memory read/write address (after any relocation and/or reclamation) and passes it through an address translation function (column 23, lines 7-23). Hence, the desired data resides in the machine resource is accessed for read or write operations using the translated address].

As to claim 18, refer to "As to claim 14."

As to claim 19, refer to "As to claim 2."

As to claims 20-21, refer to "As to claims 16-17."

As to claim 23, refer to "As to claim 1" through "As to claim 5." Further, figures 10, 11, and 12 show the address remapping between a subset of plurality of memory locations (showing OS#1, OS#2, and OS#3) to a subset of a plurality of machine memory address (MSU memory space) without rebooting the computer system (column 5, lines 46-67). This is achieved by relocation (column 16, lines 18-29) and reclamation (column 16, lines 30-50).

Moreover, Gulick et al. teach **copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses** [an operating system can directly read from another operating system's memory page. Also, one operating system instance can load data (i.e., copy from the first subset) destined for another operating system directly into the

other operating system's data area (i.e., the second subset) (column 15, lines 47-52)]. Moreover, Gulick et al. show in figure 3 that the contents of the "shared memory" of the OS#4 DRAM memory are copied to the "shared memory" segment of the MSU memory space (350). Other examples illustrating the "copying" from one memory address to a second memory space can be found in figures 4, 5, 10, 11, and 12.

As to claim 25, refer to "As to claim 23."

As to claim 27, Vishin et al. teach in their invention "Auxiliary Translation Lookaside Buffer for Assisting in Accessing Data in Remote Address Space" a method and apparatus of translating virtual addresses into physical address using a remote translation lookaside buffer (RTLB) which is implemented using a content addressable memory [figure 5 shows the translation and mapping between virtual addresses and physical addresses (column 4, lines 41-62); figure 6 shows that a CAM is used to implement a remote translation lookaside buffer (RTLB); column 4, lines 63-67; column 5, lines 1-20], and the association of the physical resource identifiers and the indices of the CAM [figure 6; column 5, lines 60-67; column 4, lines 5-10; column 5, lines 32-59; column 6, lines 1-35].

As to claim 28, refer to "As to claim 27."

As to claim 29, refer to "As to claim 27."

As to claim 30, Gulick et al. teach **copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses** [an operating system can directly read from another operating system's memory page. Also, one operating system instance can load data

(i.e., copy from the first subset) destined for another operating system directly into the other operating system's data area (i.e., the second subset) (column 15, lines 47-52)]. Moreover, Gulick et al. show in figure 3 that the contents of the "shared memory" of the OS#4 DRAM memory are copied to the "shared memory" segment of the MSU memory space (350). Other examples illustrating the "copying" from one memory address to a second memory space can be found in figures 4, 5, 10, 11, and 12.

As to claim 31, refer to "As to claim 30."

6. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Kirk, (US 5,875,464), "Computer System with Private and Shared partition in Cache."
- Van Doren, (US Patent Application Publication 2001/0037435), "Distributed Address Mapping and Routing Table Mechanism That Supports Flexible Configuration and Partitioning in a Modular Switch-Based Shared-memory Multiprocessor Computer System."
- Chi et al., (US 5,940,870), "Address Translation for Shared-memory Multiprocessor Clustering."
- Greenstein et al., (US 5,784,702), "System and method for Dynamically Performing Resource Reconfiguration in a Logically Partitioned Data Processing System."

- White et al., (US 5,721,858), "Virtual Memory Mapping Method and System for memory Management of pools of Logical Partitions for BAT and TLB Entries in a Data Processing System."
- Huber et al., (US 5,455,775), "Computer Design System for Mapping a Logical Hierarchy into a Physical Hierarchy."
- Parrish et al., (US 5,117,350), "Memory Address Mechanism in a Distributed memory Architecture."
- George et al., (US 4,51,964), "Dynamic Physical Memory Mapping and Management of Independent Programming Environments."
- Alvarez et al., (US 3,723,976), "Memory system with Logical and Real Addressing."

Conclusion

7. Claims 1-5, 8-11, 14-21, 23, 25 and 27-31 are rejected as explained above.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

February 28, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
3/2/06